Docket No.: SON-2047
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Akihiko Koh et al.

Application No.: 09/802,857

Confirmation No.: 3304

Filed: March 12, 2001

Art Unit: 2192

For: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM

Examiner: M. J. Yigdall

REPLY BRIEF

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on August 4, 2008.

All arguments presented within the Appeal Brief of May 1, 2008 are incorporated herein by reference. Additional arguments are provided hereinbelow.

Claims 27-28, 40 and 45-52 are currently pending in this application, with claims 27, 40 and 45 being independent. No claims have been allowed.

Among others, the following positions were presented in the Examiner's Answer, each of which will be addressed in turn in this Reply Brief:

ARGUMENT

1. **Rejection of claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki).**

CLAIMS 27-28 STAND OR FALL TOGETHER

Claim 27 includes *a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal.*

The Examiner's Answer contends that Sagane shows that the CPU 2 processes an interrupt function upon receipt of an interrupt request (Examiner's Answer at page 5).

In response to this contention, Figures 1 and 2 of Sagane are provided hereinbelow.

FIG. 1

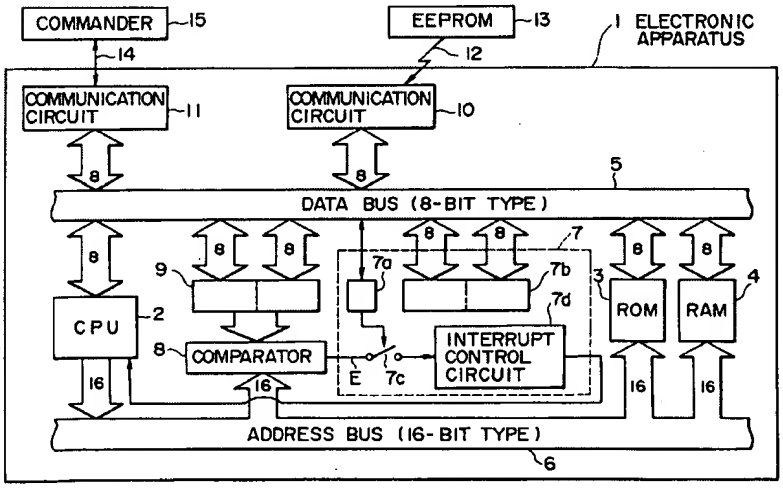


FIG. 2

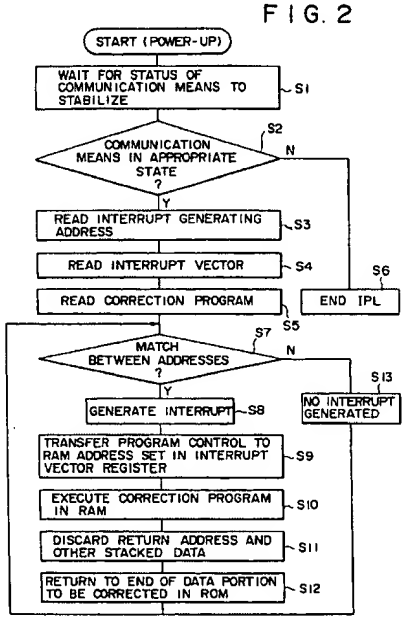


Figure 1 of Sagane appears to depict some sort of relationship between an interrupt control circuit 7d and a CPU 2. **However, the written description associated with Figure 1 of Sagane *fails* to disclose, teach, or suggest this relationship as being an interrupt.**

Here, claim 27 provides for said interrupt request signal indicating coincidence or non-coincidence of said address and said bug address, and for a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal.

Yet, *no receipt of an interrupt request signal* by the CPU 2 of Sagane can be found within Sagane.

Specifically, in case of a match between the two addresses, the **CPU** *is interrupted* to execute the correction content placed in the RAM, the correction content *taking the place of the data portion to be corrected in the ROM* (Sagane at Abstract).

Here, the Examiner's Answer refers to column 5, lines 11-16 for the teaching within Sagane of an interrupt request signal (Examiner's Answer at page 4).

Regarding column 5, lines 11-16 of Sagane, in case of a mismatch between the two addresses, ***no interrupt*** is generated and the ROM 3 is accessed (step S13) (Sagane at Figure 2, column 5, lines 11-13). If the two addresses coincide with each other, the comparator 8 supplies the interrupt control circuit 7d with a *coincidence signal E* via the switch 7c, thereby ***generating an interrupt*** (step S8) (Sagane at Figure 2, column 5, lines 13-16).

However, this passage within Sagane and a review of Figure 1 ***fails*** to disclose that the CPU 2 actually receives the coincidence signal E. As a result, Sagane ***fails*** to disclose the processing of an interrupt function by CPU 2 upon receipt of the coincidence signal E.

Moreover, Sagane ***fails*** to disclose, teach, or suggest the possible relationship between an interrupt control circuit 7d and a CPU 2 as depicted within Figure 1 is an interrupt request signal.

However, these passages within Sagane ***fail*** to disclose that the CPU processes an interrupt function *upon receipt of an interrupt request signal*.

Instead, with the interrupt generated, *control is passed on to the address latched in the interrupt vector register 7b*, i.e., the start address of the correction content in the RAM 4 (step S9) (Sagane at Figure 2, column 5, lines 16-20). This causes the correction content (program) stored in the RAM 4 to be executed (step S10) (Sagane at Figure 2, column 5, lines 20-21). **No receipt of an interrupt request signal by the CPU 2 of Sagane can be found within Figure 1 of Sagane.**

But even if receipt of an interrupt request signal by the CPU 2 of Sagane can be found within Figure 1 of Sagane, the CPU 2 processing an interrupt function upon receipt of the interrupt request signal is also ***absent*** from within Sagane.

Figures 3 and 4 of Sagane are provided hereinbelow.

FIG. 3

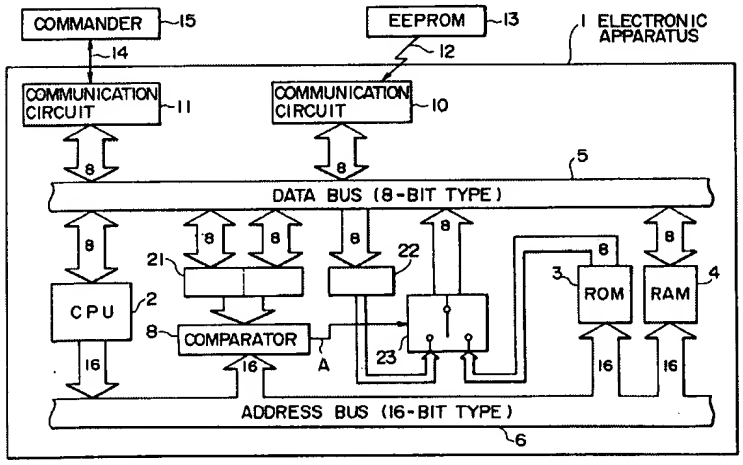


FIG. 4

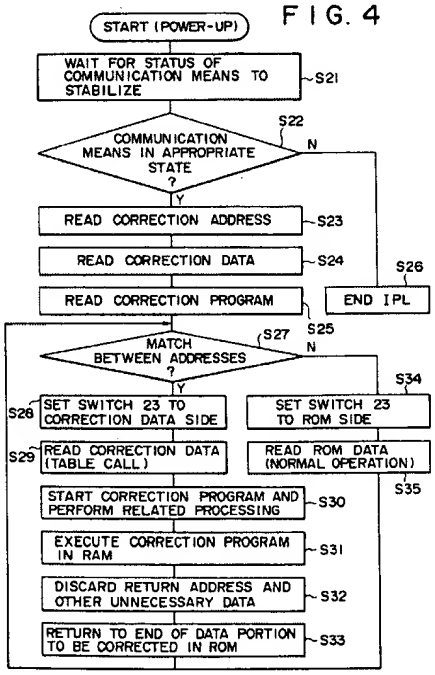


Figure 3 of Sagane fails to depict some sort of relationship between a comparator 8 and a CPU 2. **As a consequence, Figure 3 Sagane *fails* to disclose, teach, or suggest this CPU 2 as receiving an interrupt from comparator 8.**

- ***Thus, Sagane fails to disclose, teach, or suggest a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal.***

Claim 27 includes *a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.*

However, the Examiner's Answer ***readily admits*** that Sagane ***fails*** to disclose a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address (Examiner's Answer at page 5).

- ***Thus, Sagane fails to disclose, teach, or suggest a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.***

The Examiner's Answer cites Suzuki for the counter register that is admittedly absent from within Sagane.

However, Suzuki fails to disclose, teach, or suggest a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address, at least for the following reasons.

Suzuki arguably teaches that the ***PC comparison register section 20*** of the ROM correction processing circuit 24 ***compares*** a value stored in the PC latch section 22 with an address value (program counter value) of the internal bus 32 (Suzuki at column 4, lines 12-16).

Then, if these values are consistent with each other, *the PC comparison register section 20 outputs* ***an interruption request signal 34 to the CPU 14*** (Suzuki at column 4, lines 16-18).

Figure 1 of Suzuki is provided hereinbelow.

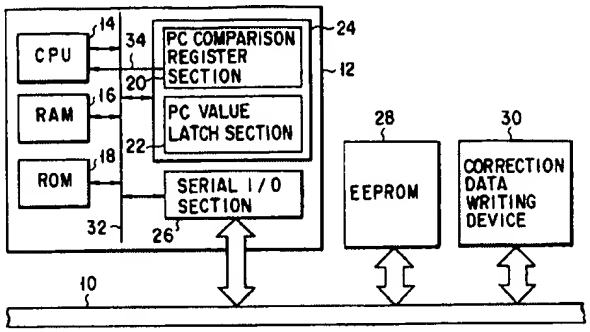


FIG. 1

Figure 2B of Suzuki is provided hereinbelow.

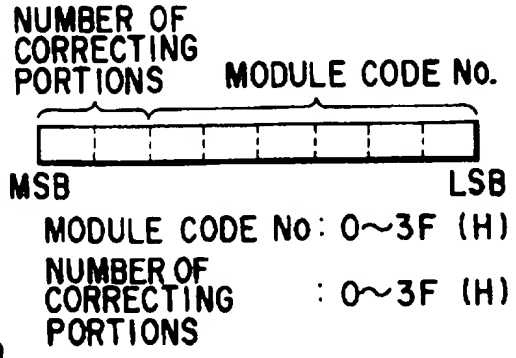


FIG. 2B

As shown in FIG. 2B, if the lower 6 bits (bit 5 to LSB) are set to a module code No. per one byte and the residual 2 bits (MSB and bit 6) are set to express the *number of correcting portions* in the module, the maximum number of modules to be dealt with becomes 64 (3F (H) to 0 (H)), and the maximum number of correcting portions is four (3 (H) to 0 (H)) (Suzuki at column 4, lines 41-45).

FIG. 3 shows an example of a data format reserved in the EEPROM 28 (hereinafter called ROM correction data area) at the time of the interruption processing (Suzuki at column 4, lines 59-61).

First of all, the *number of correcting portions* and the module code No. are stored in a head address "@0xx (H)" of the ROM correction data area (Suzuki at column 4, lines 65-67).

However, Suzuki ***fails*** to teach the number of correcting portions as representing a number of times the interrupt request signal 34 indicates a coincidence between the address and the bug address.

In particular, FIGS. 4A and 4B of Suzuki are flow charts explaining an operation when a sub-routine mode of a code No. m of the microcomputer of FIG. 1 is executed (Suzuki at column 3, lines 14-16).

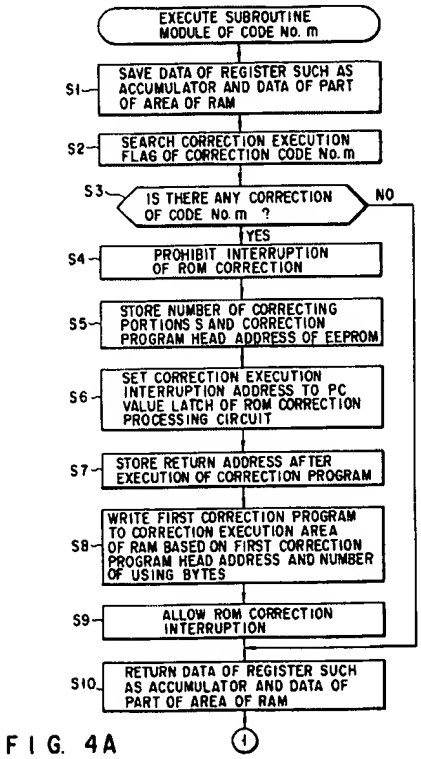


FIG. 4A

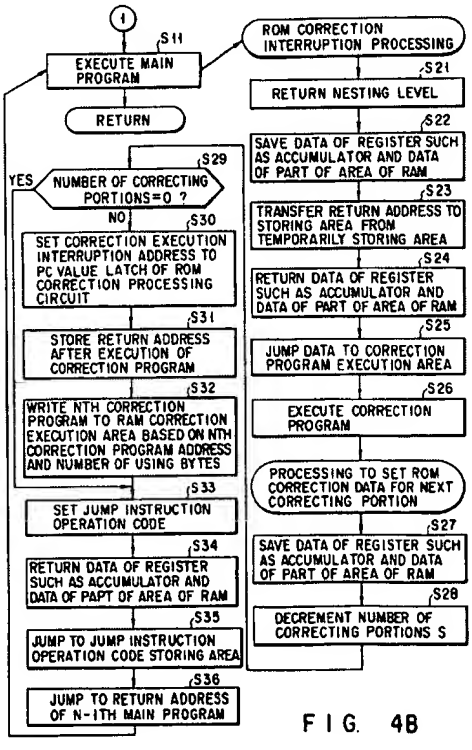


FIG. 4B

If the correction execution interruption address set in step S6 is accessed by PC (not shown) during the execution of the main program, the PC comparison register section 20 generates a *ROM correction interruption request to the CPU 14* (Suzuki at column 6, lines 28-33). The CPU 14 moves the processing to **step 21** to execute the ROM correction interruption processing on the receipt of the request (Suzuki at column 6, lines 33-35).

The stored number of correcting portions S is decremented (step S28) (Suzuki at column 6, lines 61-62). Here, what is stored within the head address "@0xx (H)" of the ROM correction data area of Suzuki is the *number of correcting portions in the module* (Suzuki at column 4, lines 41-45).

Additionally, Suzuki ***fails*** to disclose that skilled artisan would refer to the head address "@0xx (H)" of the ROM correction data area to determine the number of times the interrupt request signal 34 indicates a coincidence between the address and the bug address.

At best, if the ***number of correcting portions S is 0***, the processing goes to step S33 since there is no residual correcting portion in the subroutine module of code No. m (Suzuki at column 6, lines 65-67). Furthermore, in step S29, if the ***number of correcting portions S is not 0***, the processing goes to step S30 since there is still residual correcting portions (Suzuki at column 6, line 67 to column 7, line 2).

Here, Suzuki ***fails*** to disclose that an instantaneous review of the value contained within the head address "@0xx (H)" of the ROM correction data area of Suzuki would necessarily reveal the number of times the interrupt request signal 34 indicates a coincidence between the address and the bug address.

For example, Suzuki ***fails*** to suggest that having a value of "03" within the head address "@0xx (H)" would correlate to "three occurrences" of the interrupt request signal 34 indicating a coincidence between the address and the bug address.

- ***Thus, Suzuki fails to disclose, teach, or suggest a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.***

CLAIMS 40 STANDS OR FALLS ALONE

Sagane - The Examiner's Answer ***readily admits*** that Sagane ***fails*** to disclose a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address (Examiner's Answer at page 5).

- ***Thus, Sagane fails to disclose, teach or suggest a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address, wherein another program address indicates a location within said program memory for another of the instruction codes, and wherein said value of the counter register is incremented by 1.***

Suzuki - The Examiner's Answer cites Suzuki for the features that are deficient from within Sagane, and contends that decrementing and incrementing "are complementary operations" (Examiner's Answer at page 18).

In response, no disclosure within either Suzuki or Sagane or any other objective authority has been cited within the Examiner's Answer to support the contention that decrementing and incrementing "are complementary operations".

But even if decrementing and incrementing "are complementary operations", as the Examiner's Answer asserts, Suzuki fails to disclose, teach, or suggest that an instantaneous review of the value contained within the head address "@0xx (H)" of the ROM correction data area of

Suzuki would necessarily reveal the number of times the interrupt request signal 34 indicates a coincidence between the address and the bug address.

Instead, the Examiner's Answer contends that Suzuki teaches storing a value that represents the number of correcting portions S (Examiner's Answer at page 18).

In response, whereas Suzuki arguably discloses that the value contained within the head address "@0xx (H)" of the ROM correction data area of Suzuki expresses ***the number of correcting portions in the module***, there is ***nothing*** *within Suzuki* to disclose, teach, or suggest that the value contained within the head address "@0xx (H)" represents ***the number of times the interrupt request signal 34 indicates a coincidence between the address and the bug address***.

Here, the Examiner's Answer ***fails*** to show within Suzuki that "*the number of correcting portions in the module*" and "*the number of times the interrupt request signal 34 indicates a coincidence between the address and the bug address*" are one in the same.

Furthermore, the Examiner's Answer submits that stored value is ***DECREMENTED*** by 1 (Examiner's Answer at page 19).

However, Examiner's Answer ***fails*** to show where within Suzuki there is taught that the stored number of correcting portions S *is* ***INCREMENTED*** or that the stored number of correcting portions S ***is INCREMENTED by 1***, as claimed.

After all else, the Examiner's Answer refers to a *position counter in step S88* of Suzuki (Examiner's Answer at page 20).

In response, Suzuki arguably discloses that, then, if a ***stop target position*** of the focus lens is set (step S74), the motor ML is turned on (step S76) (Suzuki at column 9, lines 33-34).

On the other hand, if the edge is detected in step S80, ***the position counter is incremented (step S88)***, and a prediction value of a ***stop position*** is calculated (step S89) (Suzuki at column 9, lines 52-54).

Incidentally, the Examiner's Answer ***fails*** to show that "*the position counter*" is germane to "*the number of correcting portions in the module*".

- ***Thus, Suzuki fails to disclose, teach or suggest a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address, wherein another program address indicates a location within said program memory for another of the instruction codes, and wherein said value of the counter register is incremented by 1.***

2. **Rejection of claims 45-52 under 35 U.S.C. §112, second paragraph.**

Regarding the rejection 35 U.S.C. §112, second paragraph, appreciation is expressed for the indication within the Examiner's Answer at page 3 of the interpreted admission of the word "said".

3. **Rejection of claims 45-50 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal) and in view U.S. Patent No. 5,784,537 (Suzuki); and**

4. **Rejection of claims 51 and 52 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal), and in view U.S. Patent No. 5,784,537 (Suzuki), and in further view U.S. Patent No. 5,701,506 (Hosotani).**

CLAIMS 45-51 STAND OR FALL TOGETHER

Sagane - The Examiner's Answer asserts that the argument found within the Appeal Brief at pages 13-14 of an absence within Sagane of *a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal* is merely a conclusion without any supporting analysis (Examiner's Answer at page 21).

In response, this assertion is disingenuous in that Examiner's Answer itself ***readily admits*** on page 10 that "*Sagane does not expressly disclose that the central processing unit adapted to process interrupt functions of different priority levels*" (Examiner's Answer at page 10).

- ***Thus, Sagane fails to disclose, teach, or suggest a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal.***

The Examiner's Answer contends that teaches element 8 of Sagane found within Figure 1 teaches the presence of a second coincidence detecting circuit (Examiner's Answer at page 11).

In response, Figure 1 of Sagane arguably teaches the presence of a comparator 8 (Sagane at column 3, line 26).

However, Figure 1 of Sagane ***fails*** to disclose, teach, or suggest the presence of a second comparator 8.

- ***Thus, Sagane fails to disclose, teach, or suggest a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal, said central processing unit receiving said second interrupt request signal.***

Examiner's Answer itself ***readily admits*** on page 12 the Sagane does not expressly disclose a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address.

- ***Thus, Sagane fails to disclose, teach, or suggest a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address.***

Examiner's Answer itself ***readily admits*** on page 12 the Sagane does not expressly disclose that said counter register is set to 0 during said initialization processing.

- ***Thus, Sagane fails to disclose, teach, or suggest an apparatus wherein said counter register is set to 0 during said initialization processing.***

Koscal - The Final Office Action ***admits*** that Koscal does not expressly disclose that wherein said first and second interrupt request signals are input to said central processing unit as a single interruption (Final Office Action at page 18).

Suzuki - Suzuki ***fails*** to disclose the presence of different priority levels. This argument has been previously set forth within the Appeal Brief at page 14. Yet, no rebuttal to this argument can be found within the Examiner's Answer.

- ***Thus, Suzuki fails to disclose, teach, or suggest a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal.***

The Examiner's Answer contends that "a person having ordinary skill in the art could, with predictable results, implement the teachings of Suzuki so as to initialize the value to 0 (***rather than S***) in step S5, increment (***rather than decrement***) the stored value in step S28, and check whether or not the stored value is equal to S (***rather than 0***) in step S29 (Examiner's Answer at page 22).

In response, MPEP§2141 III states as follows:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in *KSR* noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Court quoting *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), stated that "'[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.'" *KSR*, 550 U.S. at ___, 82 USPQ2d at 1396.

Here, an objective rational underpinning to support the legal conclusion of obviousness is ***absent*** from within the contention found within the Examiner's Answer.

Specifically, to initialize the value to 0 (***rather than S***) in step S5 is an assertion that is unsupported by any teaching within Suzuki. For example, as shown in FIG. 2B, if the lower 6 bits (bit 5 to LSB) are set to a module code No. per one byte and the residual 2 bits (MSB and bit 6) *are set to express the* ***number of correcting portions*** *in the module*, the maximum number of modules to be dealt with becomes 64 (3F (H) to 0 (H)), and the maximum number of correcting portions is four (3 (H) to 0 (H)). (Suzuki at column 6, lines 41-45). The above-obtained ***number of correction S*** of code No. m and the head address ("0 xx (H)") of the ROM correction data area ***are stored*** (step S5) (Suzuki at Figure 4A, column 6, lines 3-5). In step S29, if the number of correcting portions S

is not 0, the processing goes to step S30 since there is still residual correcting portions (Suzuki at column 6, line 67 to column 7, line 2).

As such, the Examiner's Answer ***fails*** to provide any objective evidence that the apparatus of Suzuki would remain operable if the residual 2 bits (MSB and bit 6) are set to the value to 0 (***rather than S***), or any reason as to why the skilled artisan would have chosen to set to the value to 0 (***rather than S***).

Moreover, to increment (***rather than decrement***) the stored value in step S28 is another assertion that is unsupported by any teaching within Suzuki. In particular, within Suzuki, the stored number of correcting portions S is decremented (step S28) (Suzuki at column 6, lines 61-62).

As such, the Examiner's Answer ***fails*** to provide any objective evidence that the apparatus of Suzuki would remain operable if the stored number of correcting portions S were to be incremented (***rather than decrement***) in step S28, or any reason as to why the skilled artisan would have chosen to increment (***rather than decrement***) the stored value in step S28.

Finally, to check whether or not the stored value is equal to S (***rather than 0***) in step S29 is yet another assertion that is unsupported by any teaching within Suzuki. Within Suzuki, in step S29, *if the number of correcting portions S is not 0*, the processing goes to step S30 since there is *still residual correcting portions* (Suzuki at column 6, lines 61-62).

As such, the Examiner's Answer ***fails*** to provide any objective evidence that the apparatus of Suzuki would remain operable if the apparatus checked whether or not the stored value is equal to S (***rather than 0***) in step S29, or any reason as to why the skilled artisan would have chosen to check whether or not the stored value is equal to S (***rather than 0***) in step S29.

"It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. The references themselves must provide some teaching whereby the applicant's combination would have been obvious" (citations omitted). *In re Gorman*, 18 USPQ2d

1885, 1888 (Fed. Cir. 1991). See also *In re Dembiczak*, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999) (rejection based upon hindsight is reversed).

CLAIM 52 STANDS OR FALLS ALONE

Generally - The Examiner's Answer refers to the Decision on Request for Rehearing mailed June 21, 2007 (Examiner's Answer at page 22).

In response, the claims upon which the Decision relies have been canceled.

Sagane - The Examiner's Answer ***admits*** that Sagane ***does not*** disclose a data processing apparatus, wherein said first and second interrupt request signals are input to said central processing unit as a single interruption (Examiner's Answer at page 23).

- ***Thus, Sagane fails to disclose, teach, or suggest a data processing apparatus as set forth in claim 45, wherein said first and second interrupt request signals are input to said central processing unit as a single interruption.***

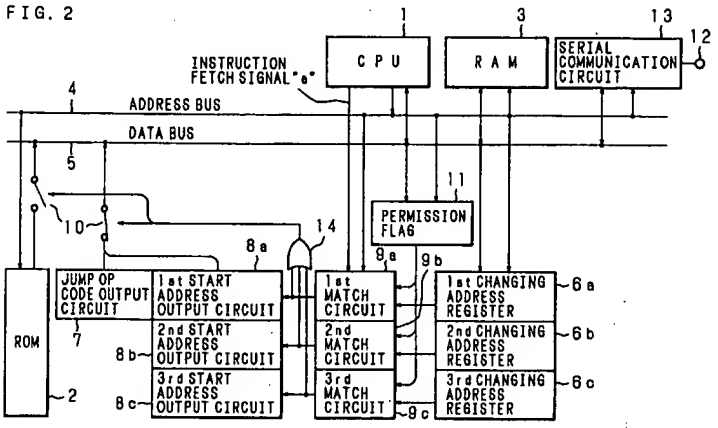
The Examiner's Answer ***admits*** that Sagane ***does not*** disclose a data processing apparatus, wherein said first and second interrupt request signals are AND'ed together to become said single interruption (Examiner's Answer at page 23).

- ***Thus, Sagane fails to disclose, teach, or suggest a data processing apparatus as set forth in claim 51, wherein said first and second interrupt request signals are AND'ed together to become said single interruption.***

Hosotani - The Examiner's Answer contends that Hosotani discloses that the signals are "AND'ed together" with predictable results (Examiner's Answer at page 24).

In response to this contention, the language of claim 52 is both clear and unambiguous. Specifically, *claim 52 is drawn to a data processing apparatus as set forth in claim 51, wherein said first and second interrupt request signals are AND'ed together to become said single interruption.*

Figure 2 of Hosotani is shown hereinbelow.



Here, claim 52 is dependent upon claim 51. Within claim 51, *said first and second interrupt request signals* ***are input to said central processing unit*** *as a single interruption.*

Hosotani arguably teaches that *the CPU 1* is also connected, via the address bus 4 and a signal line of an instruction fetch signal a, to the *first to third match circuits 9a to 9c* that respectively compare the change addresses with the address on the address bus 4 in synchronism with the output timing of the instruction fetch signal a from *the CPU 1*, and output signals indicating the results of the comparisons (a "1" level indicates an address match, and a "0" level indicates an address mismatch) (Hosotani at column 4, lines 46-53).

Hosotani ***fails*** to disclose, teach, or suggest the signals from the first to third match circuits 9a-9c ***being input to CPU 1***.

No rebuttal regarding the **absence** of the signals from the first to third match circuits 9a-9c ***being input to CPU 1*** can be found within the Examiner's Answer.

- ***Thus, Hosotani fails to disclose, teach, or suggest a data processing apparatus wherein said first and second interrupt request signals are input to said central processing unit as a single interruption.***

Hosotani ***fails*** to disclose, teach, or suggest the output of the 0R circuit 14 being connected to a connection control means 10.

Instead, ***the output of the 0R circuit 14 is connected to a connection control means 10*** which selects either the mask ROM 2 or a jump op code output circuit 7 and first to third start address output circuits 8a-8c for connection to the data bus 5 in accordance with the output level of the OR circuit 14 (which outputs a "1" level when the result of comparison from any one of the match circuits 9a-9c indicates a match, and a "0" level when all the comparison results indicate a mismatch) (Hosotani at column 4, line 61, to column 5, line 2).

- ***Thus, Hosotani fails to disclose, teach, or suggest a data processing apparatus wherein said first and second interrupt request signals are AND'ed together to become said single interruption.***

RELATED PROCEEDINGS APPENDIX

Within the Decision on Appeal mailed October 31, 2006, the Board of Patent Appeals and Interferences (the Board) concluded that the Examiner had made a *prima facie* case of obviousness and, thus, sustained the rejection of prior claims 13-25 under 35 U.S.C. §103.

Within the Decision on Rehearing mailed on June 21, 2007, the Board has maintained its earlier conclusion rendered in the Decision on Appeal of October 31, 2006 regarding claims 13-25.

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

CONCLUSION

There is no concession as to the veracity of Official Notice, if taken in any Office Action. An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

The prior art of record fails to disclose, teach or suggest all the features of the claimed invention.

For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained.

Therefore, a reversal of the rejection of December 28, 2007 is respectfully requested.

If any additional fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: September 5, 2008

Respectfully submitted,

By 40,290

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